AMENDMENTS TO THE CLAIMS:

Please cancel claims 12 and 19, without prejudice or disclaimer of subject matter. This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1 to 12. (Cancelled).

13. (Previously Presented) A video signal processing apparatus comprising:

a plurality of line memories to which in sequence video signal data inputted is written on a line-by-line basis;

a timing controller for controlling a timing to write the video signal data to the plurality of line memories and a timing to read the video signal data from the plurality of line memories;

a computation output portion for computing the video signal data read from the plurality of line memories and outputting video signal data differing in resolution which is determined by a pixel count in the horizontal direction and a line count in the vertical direction;

a reference pixel count decision unit which decides a reference pixel count in the horizontal direction of the video signal data obtained from the computation output portion, by letting a difference be a specified period of time which is determined depending on a conversion rate of the resolution of the video signal data, wherein the difference is a difference between an elapsed period of time for a specified number of lines of the video signal data inputted and an elapsed period of time for a line count corresponding to the specified number of lines of the video signal data obtained from the computation output portion;

a counting unit which counts the specified period of time; and

a pixel count variation unit which varies from the reference pixel count the pixel count in the horizontal direction of the video signal data obtained from the computation output portion if the count of the counting unit is equal to or smaller than the specified period of time.

14. (Previously Presented) A video signal processing apparatus according to claim 13, wherein the pixel count variation unit provides the pixel count in the horizontal direction of the video signal data obtained from the computation output portion, with a certain number increase over the reference pixel count, if the count of the counting unit is equal to or smaller than the specified period of time.

15. (Previously Presented) A video signal processing apparatus according to claim 14, wherein the pixel count variation unit varies the pixel count in units of the certain number smaller than that of one screen-full of lines in the vertical direction of the video signal data obtained from the computation output portion.

16. (Previously Presented) A video signal processing apparatus according to claim 15, wherein the reference pixel count decision unit is operable to decide the reference pixel count during vertical blanking interval of the video signal data inputted, and wherein the pixel count variation unit is operable to use the reference pixel count for the video signal data to be obtained from the computation output portion.

17. (Previously Presented) A video signal processing apparatus according to claim 13, wherein the plurality of line memories include at least three line memories, and wherein, while the video signal data is written to a first line memory, the video signal data is read from a second and third line memory.

18. (Previously Presented) An integrated circuit comprising the video signal processing apparatus according to claim 13.

19. (Cancelled).

20. (Previously Presented) A method of processing a video signal for a video signal processing apparatus which comprises a plurality of line memories to which in sequence video signal data inputted is written on a line-by-line basis, a timing controller for controlling a timing

to write the video signal data to the plurality of line memories and a timing to read the video signal data from the plurality of line memories, and a computation output portion for computing the video signal data read from the plurality of line memories and outputting video signal data differing in resolution which is determined by a pixel count in the horizontal direction and a line count in the vertical direction, the method of processing a video signal comprising:

deciding a reference pixel count in the horizontal direction of the video signal data obtained from the computation output portion, by letting a difference be a specified period of time which is determined depending on a conversion rate of the resolution of the video signal data, wherein the difference is a difference between an elapsed period of time for a specified number of lines of the video signal data inputted and an elapsed period of time for a line count corresponding to the specified number of lines of the video signal data obtained from the computation output portion;

counting the specified period of time; and

varying from the reference pixel count the pixel count in the horizontal direction of the video signal data obtained from the computation output portion if the count is equal to or smaller than the specified period of time.

21. (Previously Presented) A method of processing a video signal according to claim 20, further comprising providing the pixel count in the horizontal direction of the video signal data obtained from the computation output portion, with a certain number increase over the reference pixel count, if the count is equal to or smaller than the specified period of time.

22. (Previously Presented) A method of processing a video signal according to claim 21, further comprising varying the pixel count in units of the number smaller than that of one screen-full of lines in the vertical direction of the video signal data obtained from the computation output portion.

23. (Previously Presented) A method of processing a video signal according to claim 22, further comprising:

deciding the reference pixel count during vertical blanking interval of the video signal data inputted; and

using the reference pixel count for the video signal data to be obtained from the computation output portion.

24. (Previously Presented) A method of processing a video signal according to claim 20, wherein the plurality of line memories include at least three line memories, and wherein, while the video signal data is written to a first line memory, the video signal data is read from a second and a third line memory.